

**REMARKS**

Claims 1-22 were examined and reported in the Office Action. Claims 1-22 are rejected. Claims 1, 3, 7, 12, 17 and 19 are amended. Claims 1-22 remain.

Applicant requests reconsideration of the application in view of the following remarks.

**I.      Double Patenting**

It is asserted in the Office Action that claims 1-22 are rejected under the judicially created doctrine of double patenting over claims 1-19 of U. S Patent No. 6,721,815 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The Office Action states that a timely filed terminal disclaimer in compliance with 37 CFR 1.32(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned. Applicant submits a terminal disclaimer with this response.

**II.     35 U.S.C. §102(e)**

It is asserted in the Office Action that claims 1-5, 7-10, 12-15, and 17-21 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,349,354 issued to Garney ("Garney"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged

as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (*In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a]n apparatus comprising: a host controller to generate a transaction schedule, the transaction schedule including a plurality of transactions, the plurality of transactions are stored in a plurality of data structures, where the plurality of data structures are isochronous transaction descriptors (iTDs) wherein the host controller executes the transactions that are initialized and the plurality of data structures each contain a pointer to a next initialized transaction, and, the host controller daisy chains partially initialized iTDs into a single classic frame."

Applicant's amended claim 7 contains the limitations of "[a] method comprising: determining a starting micro-frame; receiving buffer data; creating at least one isochronous transaction descriptor (iTD) based on the starting micro-frame and buffer data; inserting the at least one iTD into a frame list, wherein at least one partially initialized iTD is daisy chained with at least one other partially initialized iTD into at least one buffer and inserted into a single classic frame."

Applicant's amended claim 12 contains the limitations of "[a]n apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising: determining a starting micro-frame; receiving buffer data; creating at least one isochronous transaction descriptor (iTD) based on the starting micro-frame and buffer data; inserting the at least one iTD into a frame list, wherein at least one partially initialized iTD is daisy chained with at least one other partially initialized iTD into at least one buffer and inserted into a single classic frame."

Applicant's amended claim 17 contains the limitations of "[a] system comprising: a host controller coupled to a bus, the host controller generates a transaction schedule, the transaction schedule including a plurality of transactions, the plurality of transactions are stored in a plurality of data structures; and a device coupled to the bus,

wherein the host controller executes transactions that are initialized, the plurality of data structures each contain a pointer to a next initialized transaction, the plurality of data structures are isochronous transaction descriptors (iTDS), and partially initialized iTDs are daisy chained into a single classic frame.”

It is asserted in the Office Action that Garney teaches “the at least one iTD contains one of initialized transactions and initialized and non-initialized transactions (col. 2 lines 19-61 and col. 5lines 1-40).” (Office Action, page 5, third paragraph). Applicant asserts, however, that nowhere in Garney is it taught, disclosed or suggested that partially iTDs are daisy chained into a single classic frame. Moreover, Garney does not teach, disclose or suggest dealing with anything but normal TDs. (Garney, col. 6, lines 8-13; “Use of a normal isochronous TD results in retirement of the TD after each transaction, therefore the host controller driver will likely want to link several isochronous TDs to the delay QH. If the isochronous transaction can be made persistent, e.g., indefinitely retrievable, a single isochronous TD may be used.”)

Therefore, since Garney does not disclose, teach or suggest all of Applicant’s amended claims 1, 7, 12 and 17 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Garney. Thus, Applicant’s amended claims 1, 7, 12 and 17 are not anticipated by Garney. Additionally, the claims that directly or indirectly depend on claims 1, 7, 12 and 17, namely claims 2-5, 8-10, 13-15, and 18-21, respectively, are also not anticipated by Garney for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(e), rejections for claims 1-5, 7-10, 12-15, and 17-21 are respectfully requested.

### **III. Claims Rejected under 35 U.S.C. §103(a)**

It is asserted in the Office Action that claims 6, 11, 16, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Garney in view of no other prior art. Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 “[t]o establish a *prima facie* case of obviousness, three

basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 6 depends on amended claim 1. Applicant's claim 11 depends on amended claim 7. Applicant's claim 16 depends on amended claim 12. Applicant's claim 22 depends on amended claim 17. Applicant has addressed Garney regarding claims 1, 7, 12 and 17 above in section II.

Further, it is asserted in the Office Action that it "would have been obvious for one of ordinary skill in the art at the time of the invention to utilize notoriously well known concept of variable sized buffers into Garney's system so that increased efficiency is achieved during movement of large amounts of data." Applicant respectfully queries as to sources in the art of USB scheduling of iTDs, known before the time of invention, are variably sized buffers used?

Regardless, as asserted above, Garney does not teach, disclose or suggest "partially initialized iTDs are daisy chained into a single classic frame." Since Garney does not teach, disclose or suggest all the limitations of Applicant's amended claims 1, 7, 12 and 17, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 7, 12 and 17 are not obvious over Garney in view of no other prior art since a *prima facie* case of obviousness has not

been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 7, 12 and 17, namely claims 6, 11, 16, and 22, respectively, would also not be obvious over Garney in view of no other prior art for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 6, 11, 16, and 22 is respectfully requested.

**CONCLUSION**

In view of the foregoing, it is submitted that claims 1-22 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: May 11, 2005  
By \_\_\_\_\_  
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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 11, 2005.

  
Jean Svoboda